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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GRAHAM, ANDREW R	
ART UNIT	**PAPER NUMBER**
2644	9

DATE MAILED: 10/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/521,641	FREED ET AL.	
	Examiner	Art Unit	
	Andrew Graham	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on March 8, 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to because they fail to meet several of the requirements of CFR § 1.84. The following requirements have not been met:

- *§ 1.84 (l) Character of lines, numbers, and letters:*

Every line, number, and letter must be durable, clean, black (except for color drawings), sufficiently dense and dark, and uniformly thick and well-defined. The weight of all lines and letters must be heavy enough to permit adequate reproduction.

- *§ 1.84 (p)(3) Numbers, letters, and reference characters:*

Numbers, letters, and reference characters must measure at least .32 cm. (1/8 inch) in height. They should not be placed in the drawing so as to interfere with its comprehension.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

A substitute specification is required pursuant to 37 CFR 1.125(a) because the margin at the top of the specification is insufficient. The top line of the specification is unreadable because of the manner in which the papers are physically entered into the file

wrapper. Each sheet, other than the drawings, must include a top margin of at least 2.0 cm. (3/4 inch), pursuant to MPEP 608.01.

A substitute specification filed under 37 CFR 1.125(a) must only contain subject matter from the original specification and any previously entered amendment under 37 CFR 1.121. If the substitute specification contains additional subject matter not of record, the substitute specification must be filed under 37 CFR 1.125(b) and (c).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, and 10-13 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Wei (USPN 6029133) in view of Fielder et al (USPN 5109417). Hereafter, "Fielder et al" will simply be referred to as "Fielder".

Wei discloses a synthesizer that recursively derives frames of waveforms. The system provides the pitch frequency (45) for each audio frame as well as the magnitude (60), time durations of each frame (55), and ending phase (50) to second order resonators (40) that generate the corresponding harmonics, which are then summed and shaped

by a gain circuit (70) according to an input description of the original audio signal (col. 3, lines 14-24 and col. 5, lines 22-65). Figures 2a and 2b illustrate the recursive structure of the digital oscillators (col. 5, lines 31-62). These devices, and the combination of their outputs read on "A method of performing additive synthesis of digital audio signals in a recursive digital oscillator". As can be seen in Figure 1, the inputs for the system include the pitch frequency (15) for the current synthesizing frame, the ending phase information (25) for the harmonics in each frame, and the magnitudes (35) of each of the harmonics in each frame (col. 3, line 67 and col. 4, lines 1-14). This information as input reads on "receiving digital audio signal frames wherein each digital audio signal frame includes a set of frequency, amplitude, and phase components represented as coefficients of variables in a mathematical expression". The merging of the waveforms reads on "performing additive synthesis with said converted frequency coefficients" (col. 7, lines 46-54).

While Wei discloses the general structure synthesizing the digital waves, Wei does not specify:

- that the frequency coefficients are linearly remapped to bias audio reproduction accuracy toward low frequency signals

Fielder discloses a digital audio synthesis system that includes adaptive bit allocation for the various frequency channels within an audio signal. The digital versions of the signals are initially processed as 16 bit words padded with zeros (col. 14, lines

61-65). A non-uniform quantizer bank (108) then encodes the different, distinct frequencies of the audio signal with a pair of exponents, a minimum bit length, and a set of bits that may selectively be allocated to the representations of each frequency band (col. 19, lines 3-12). The minimum bit lengths for the coefficients representing each frequency band are shown in Table 1, including 8 and 5 bits for the lower frequency bandwidths (col. 21, lines 5-8 and col.38, lines 12-68). These bandwidths are initiated with a higher number bits than the higher frequency bands, which as can be seen in the table, receive between 2 and 4 bits minimum. The quantizer (108) also includes an adaptive bit allocation section (106), which includes the capability of assigning additional bits to the bandwidth coefficients (col. 22, lines 59-68). The allocation process involves preference for bandwidths with the highest spectral energy, which would also favor lower frequency components present in an input signal, extending the initial bit-enhanced status of such components. Collectively, this bit quantization process reads on "forming converted frequency coefficients by linearly remapping of bits of said frequency coefficient representation to bias audio reproduction accuracy toward low frequency signals". It is noted that the phrase "linearly re-mapping" is broad in scope and has been interpreted in this rejection accordingly.

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to include the bit encoding and quantization scheme of Fielder in the recursive digital filter of Wei.

The motivation behind such a modification would have been the reduction in bits used to represent the signal. The modification would have been particularly desirable because the bit allocation plays a significant role in signal intelligibility involved with the lower frequencies, and the disclosed encoding minimizes the bit length, but does not compromise the quality of these components.

Regarding **Claim 2**, the exponent representation of Fielder is a floating point representation, which reads on "the step of defining said frequency coefficient representation with an exponent characterizing a floating point range extension" (col. 19, lines 14-58).

Regarding **Claim 3**, the exponent in the arrangement of Wei always represents the number of right shifts necessary for the true value of the floating point quantity to be obtained (col. 19, lines 54-58). This reads on "the step of specifying said exponent to correspond to a right shift amount necessary to correct for precision limitations". Regarding the coefficient representation lengths, as discussed previously, Table 1 shows the minimum number of bits to be allocated for each frequency bandwidth coefficient. Regarding adaptively allocated bits, Fielder teaches an embodiment wherein a maximum number of 4 bits are added to each frequency coefficient however, it is also disclosed that this number may be altered with the respective expected effects upon coding accuracy and bit rate (col. 23, lines 6-12). It is also noted that the initially quantized

signals used 16 bits (col. 12, lines 47-63). This, in regards to the bit representation of the coefficients, reads on "introduced by limiting re-mapping coefficients to 16 bits".

Regarding **Claim 5**, Figure 2a of Fielder illustrates the use of a digital signal processor (202) in the system, which reads on the method is implemented "utilizing a digital signal processor" (col. 12, lines 64-68).

Regarding **Claim 10**, please refer to the like teachings of Claims 1 and 5, noting the hardware implementations of the system of Fielder shown in Figures 2a-2e and 3a-3b.

Regarding **Claim 11**, please refer to the like teachings of Claim 1, and the inherent "identification" of inputs received in the system of Wei.

Regarding **Claim 12**, please refer to the like teachings of Claim 2. Regarding **Claim 13**, please refer to the like teachings of Claim 3.

Claim 4 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Wei in view of Fielder as applied above, and in further view of Chen (USPN 5729577).

As detailed above, Wei discloses a recursive digital oscillator, and Fielder discloses a method for reducing the bit rate of a representation of a signal without compromising the quality of the frequency components of the signal. Both Wei and Fielder disclose the use of digital signal processors with their systems.

However, Wei in view of Fielder do not specify:

- that the processor is a 16 bit fixed point processor

Chen discloses a signal processor with an improved efficiency using a recursive structure and outputting sinusoids at arbitrary frequencies. The processor used in the system of Chen is a 16 bit fixed point processor (col. 2, lines 59-60). Chen lists the advantages of using such a processor, which includes a fewer number of processing steps for providing an output arbitrary frequency signal and also a near zero processing latency (col 2, lines 60-66). This reads on "implementing utilizing a 16 bit fixed point processor".

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to include a 16 bit fixed processor as disclosed by Chen in the synthesis system of Wei in view of Fielder. The motivation behind such a modification would have been the processing advantages of using such a processor, as listed by Chen, including the reduction in processing steps and the minimal processing latency.

Claims 6-8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Wei in view of Fielder as applied above, and in further view of Dowling (USPN 6163836).

As detailed above, Wei discloses a recursive digital oscillator, and Fielder discloses a method for reducing the bit rate of a representation of a signal without compromising the quality of the frequency components of the signal. Both Wei and Fielder disclose the use of digital signal processors with their systems.

However, Wei in view of Fielder do not specify:

- that the processor is a field programmable gate array

Dowling discloses a processor with programmable addressing modes. One particular embodiment of the system of Dowling is a field programmable gate array (col. 15, lines 12-21). Such a processor involves the advantages of a hardware description language code that is used for both verification and implementation, as well as special circuitry to implement common arithmetic functions Col. 16, lines 32-49). This embodiment reads on "implemented utilizing a field programmable gate array".

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to execute the synthesis system of Wei in view of Fielder on the processor of Dowling. The motivation behind such a modification would have been the use of the same description language code and the specialized circuitry as taught by Dowling.

Regarding **Claim 7**, another embodiment of the system of Dowling is a Very Long Instruction Word processor, which reads on "implemented using a Very Long Instruction Word processor" (col. 17, lines 20-65).

Regarding **Claim 8**, Dowling also discloses the use and known advantages of Reduced Instruction Set Computers, which reads on "implemented utilizing a Reduced Instruction Set Computer" (col. 1, lines 21-65).

Claim 9 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Wei in view of Fielder as applied above, and in further view of Capps et al (USPN 4910699). Hereafter, "Capps et al" will simply be referred to as "Capps".

As detailed above, Wei discloses a recursive digital oscillator, and Fielder discloses a method for reducing the bit rate of a representation of a signal without compromising the quality of the frequency components of the signal. Both Wei and Fielder disclose the use of digital signal processors with their systems.

However, Wei in view of Fielder do not specify:

- that the processor is a Residue Number System processor

Capps discloses an optical computer that includes binary to residue conversion and deconversion. Optical computers are disclosed as being readily supportive of complex global interconnect structures, while their electronic counterparts are not (col. 4, lines 56-68 and col. 5, lines 1-2). Capps also discloses that residue number processing more optimally matches optical technology, and significant processing speeds may potentially be obtained wit such systems (col. 5, lines 10-18). The system of Capps includes binary to residue converter (2) to enable residue number processing of binary data using optical processors, and residue to binary converters for converting the data back to a more local, universal binary form (Figure 1). This processor reads on "implemented utilizing a Residue Number System processor.

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to utilize the optical processor and converters of Capps in the system of Wei in view of Fielder. The motivation behind such a modification would have been the enhanced processing speed provided by the parallel optical processors, and the conversion means that would have enabled the input and outputs of the system to be in the more common and therefore prominently useful binary format.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Graham whose telephone number is (703) 308-6729. The examiner can normally be reached on Monday-Friday (7:30-4:30), excluding alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Isen, can be reached at (703) 305-4386. The fax number for the organization where this application or proceeding is assigned is 703-872-9314 for regular communications, and 703-872-9315 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

FORESTER W. ISEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Andrew Graham
Examiner
A.U. 2644

ag
October 20, 2003